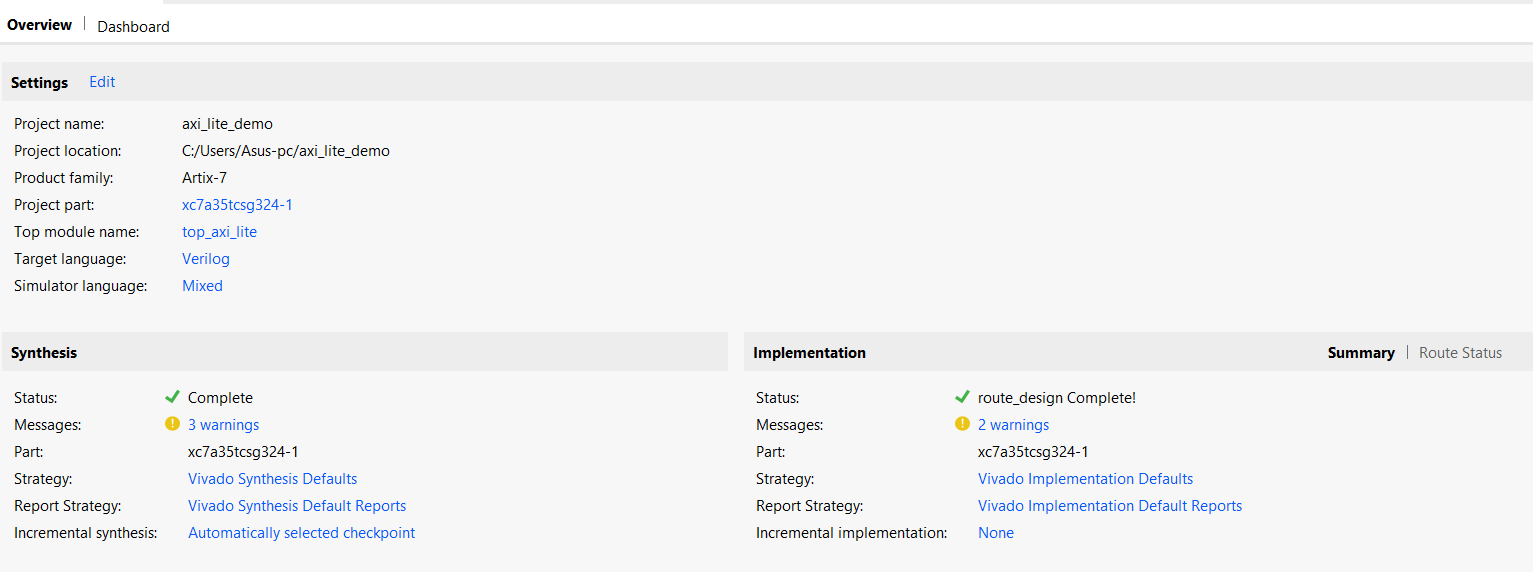
AXI4-Lite Master/Slave Simulation Results

Figure . Synth and implementation



This project currently does not include an XDC constraint file, which results in warning messages during implementation and prevents bitstream generation

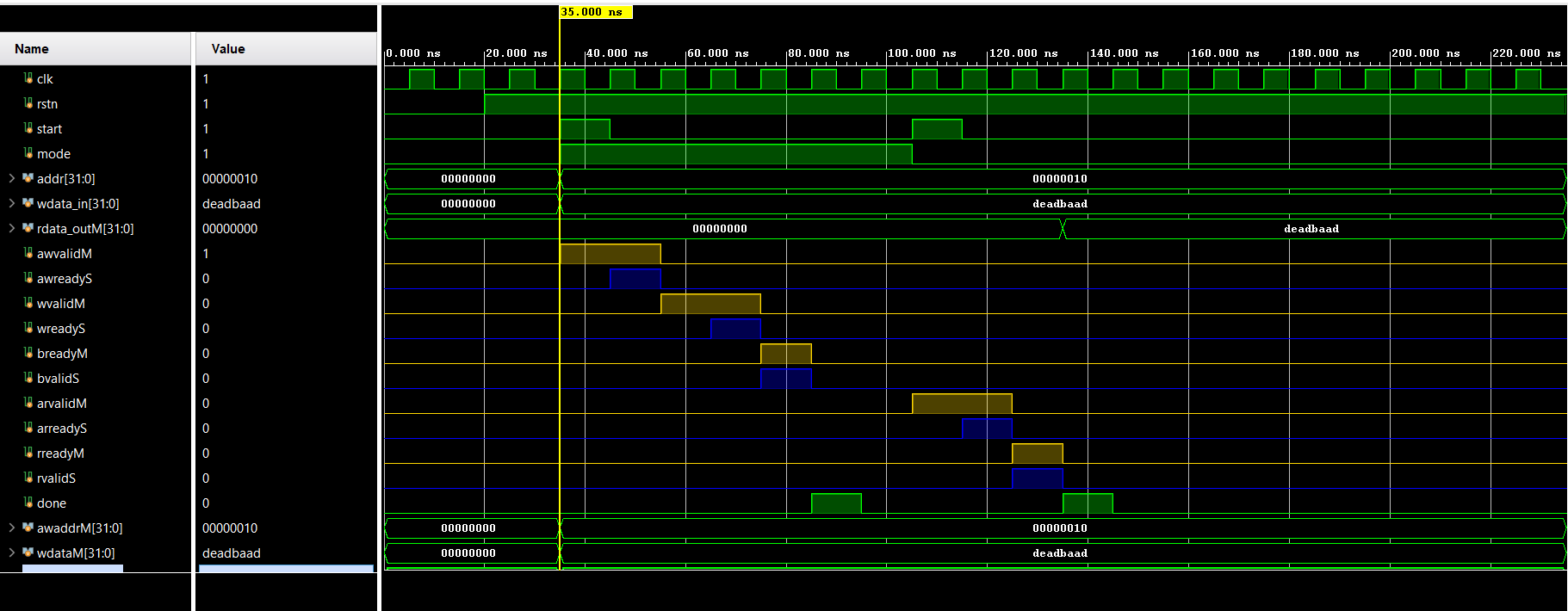
In this figure, we can clearly observe the handshake process.  
At time 35 ns, **AWVALID** is asserted by the master, followed by **AWREADY** from the slave in the next cycle.  
Subsequently, at time 55 ns, the master asserts **WVALID**, and the slave responds with **WREADY** one cycle later.  
Finally, we see **BREADY** from the master and **BVALID** from the slave, completing the write transaction.

Figure .master slave handshakes

A similar sequence is observed for the read transaction:  
At time 105 ns, the master asserts **ARVALID**, and the slave responds with **ARREADY** in the following cycle. The master then asserts **RREADY**, and the slave responds with **RVALID**, completing the read handshake.

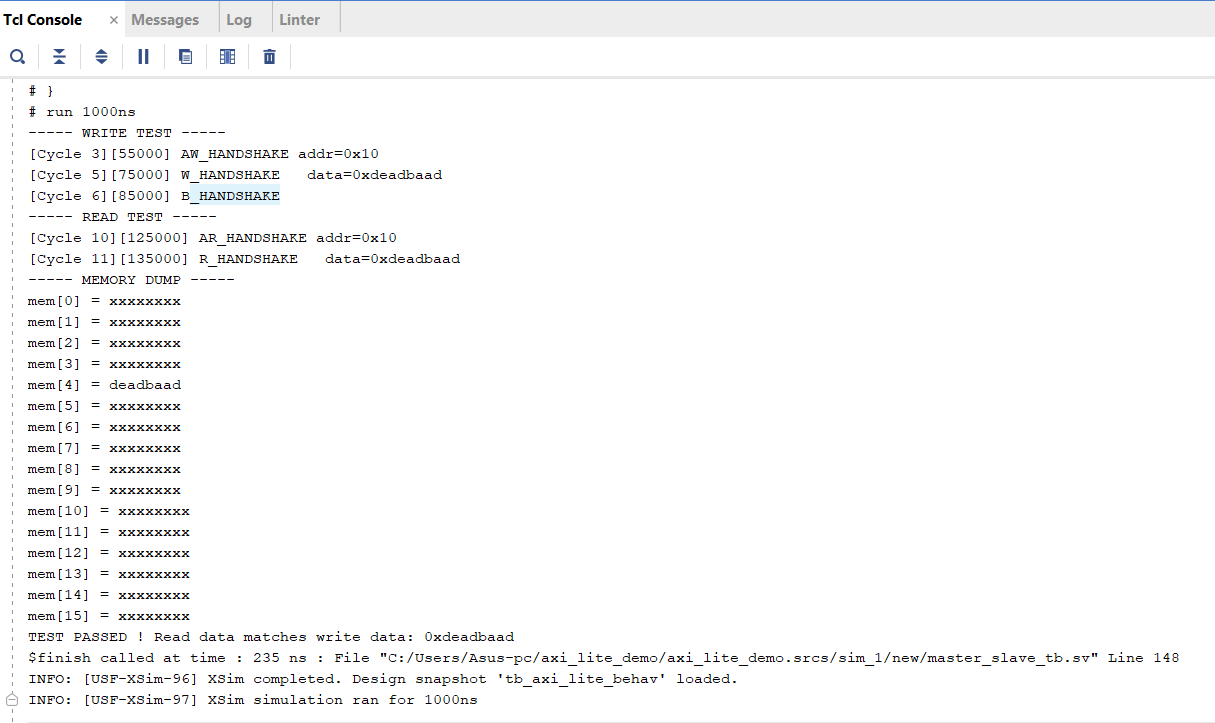


Figure .prints from testbench

The figure above shows the printed simulation output. It includes the memory contents, demonstrating that the write and subsequent read operations were performed correctly. The write transaction stores the expected data at the specified address, and the read transaction successfully retrieves the same value, confirming correct AXI-Lite slave functionality.

The simulation setup is identical to the previous case, except that here the DUT is instantiated as the top-level module.

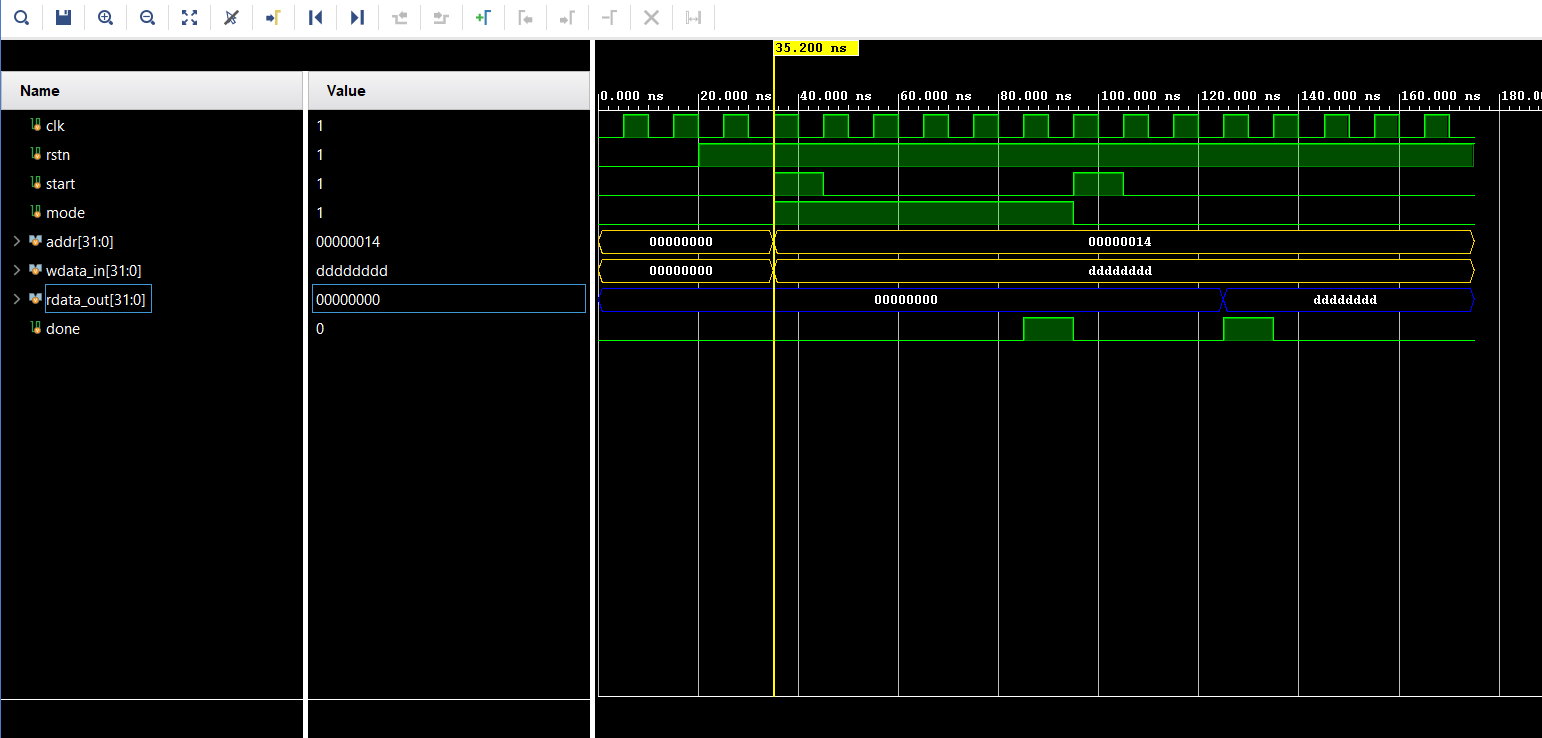


Figure .top level module testbench